T.T.L. QUADRUPLE 2-INPUT NAND GATES

FJH131 FJH131A FJH136

Correspond to 74 Series types 7400N, 6400N

TENTATIVE DATA

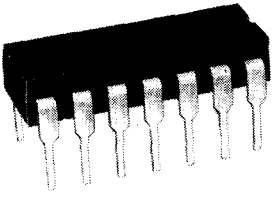
These devices are transistor-transistor logic quadruple 2-input NAND gates in the FJ series of integrated circuits. The FJH131 corresponds to '74 Series' type 7400N, the FJH136 corresponds to '64 Series' type 6400N.

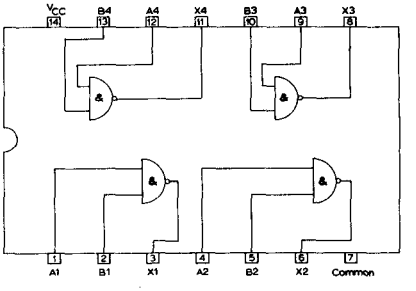
QUICK REFERENCE DATA		
Supply voltage (nominal)	5.0	V
Fan-out (max.)	10	
Noise immunity (typ.)	1.0	V
(min.)	0.4	V
Operating temperature range FJH131/1A	0 to +70	^{o}C
FJH136	-40 to +85	^{o}C
Propagation delay (typ.)	13	ns
Average power dissipation (50% duty cycle, $T_{amb}=25^{o}C$)	10	mW
Fan-in	2	

Unless otherwise stated data applies to individual gates

OUTLINE

Conforms to J.E.D.E.C. TO-116 (see page 4)
FJH131 - 14-lead all plastic dual-in-line package
FJH131A - 14-lead hermetic-in-plastic dual-in-line package
FJH136 - 14-lead all plastic dual-in-line package





LOGIC FUNCTION

The logic function of the gate is a NAND when the most positive signal voltage is a '1' and a NOR when the most positive signal voltage is a '0'. All inputs to the gate are to be 'High' in order for the output to be 'Low'. A 'Low' input to any gate input will give the output 'High'.

DESIGN DATA (Maximum adverse operating conditions assumed)

		Min.	Nom.	Max.	
Temperature					
Operating ambient	FJH131/1A	0	-	70	°C
	FJH136	-40	-	85	°C
Supply					
Supply voltage	FJH131/1A	4.75	-	5.25	V
	FJH136	4.5	-	5.5	V
Supply current (output 'Low') per gate		-	3.0	-	mA
Supply current (output 'High') per gate		-	1.0	-	mA
Inputs					
Voltage for 'High' input state	S.N.I. = 0	2.0	-	-	V
	S.N.I. = 0.4V	2.4	-	-	V
*Current for 'High' input state (each input)		-	-	40	μA
Voltage for 'Low' input state	S.N.I. = 0	-	-	0.8	V
	S.N.I. = 0.4V	-	-	0.4	V
**Current for 'Low' input state					
Outputs					
Voltage for 'High' output state		2.4	-	-	V
Output resistance in 'High' output state		-	100	-	Ω
Voltage for 'Low' output state		-	-	0.4	V
Output resistance in 'Low' output state		-	12	-	Ω
Current capability at 'Low' output state		-	-	16	mA
Fan-out		-	-	10	

Truth Table (for two input terminals)

Input 1	Input 2	Output
Low	Low	High
High	Low	High
Low	High	High
High	High	Low

Performance

Signal noise immunity	0.4	1.0	-	V
Average propagation delay time (C_L = 15pF)	-	13	-	ns

This is equivalent to a propagation delay time to the 'Low' state of 8.0ns and to the 'High' state of 18ns.

*The 'High' state normally corresponds to a voltage level between 2.4 and 5.25V.
**The 'Low' state normally corresponds to a voltage level between 0 and 0.4V.

CHARACTERISTICS (Supply voltage = 5.0V, $T_{amb} = 25^{o}C$)

		Min.	Typ.	Max.	
V_{TH} 'Low'	Input threshold voltage for 'Low' input state ($V_{out} = 2.4V$, $I_{out} = -400\mu A$)	0.8*	-	-	V
V_{TH} 'High'	Input threshold voltage for 'High' input state ($I_{out} = 16mA$, $V_{out} = 0.4V$)	-	-	2.0*	V
V_{out} 'Low'	Output voltage for 'Low' output state ($V_{in} = 2.0V$, $I_{out} = 16mA$)	-	0.23	0.4*	V
V_{out} 'High'	Output voltage for 'High' output state ($V_{in} = 0.8V$, $I_{out} = -400\mu A$)	2.4*	3.0	-	V
I_{in} 'Low'	Input current for 'Low' input state ($V_{in} = 0.4V$, $I_{out} = 0$)	-	-	1.6*	mA
I_{in} 'High'	Input current for 'High' input state (each input) ($V_{in} = 2.4V$, $I_{out} = 0$, other inputs = 0V)	-	-	40*	μA
I_{out} 'High'	Leakage current into the 'High' state output at $V_{out} = 6.7V$ ($V_{in} = 0$)	-	-	300	μA
I_{out} s/c 'High'	Short circuit output current for 'High' output state ($V_{in} = 0$, o/p grounded)	18*	-	55*	mA
t_{pd0}	Propagation delay time to logical '0' level (Fan-out = 10, $C_L = 15pF$)	-	8.0	15	ns
t_{pd1}	Propagation delay time to logical '1' level (Fan-out = 10, $C_L = 15pF$)	-	18	29	ns

*These are the characteristics which are recommended for acceptance testing purposes.

NOTE

C_L = Total capacitance of driven gates including wiring capacitance.

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

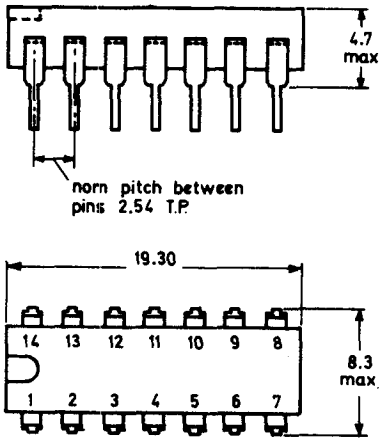
Maximum positive supply voltage (pin 14)	7.0	V
Maximum continuous input voltage (pins 1, 2, 4, 5, 9, 10, 12, 13)	5.5	V
Maximum continuous voltage applied to output (applied through $R_L \geq 270\Omega$) (Pins 3, 6, 8, 11)	7.0	V
Maximum negative transient input voltage ($t_p = 20ns$, $f = 5.0MHz$, $R_s \geq 75\Omega$)	-2.0	V

Temperature

T_{stg} min.	-65	°C
T_{stg} max.	150	°C
T_{amb} operating range FJH131/1A	0 to +70	°C
T_{amb} operating range FJH136	-40 to +85	°C

OUTLINE AND DIMENSIONS

Conforms to J.E.D.E.C. TO-116

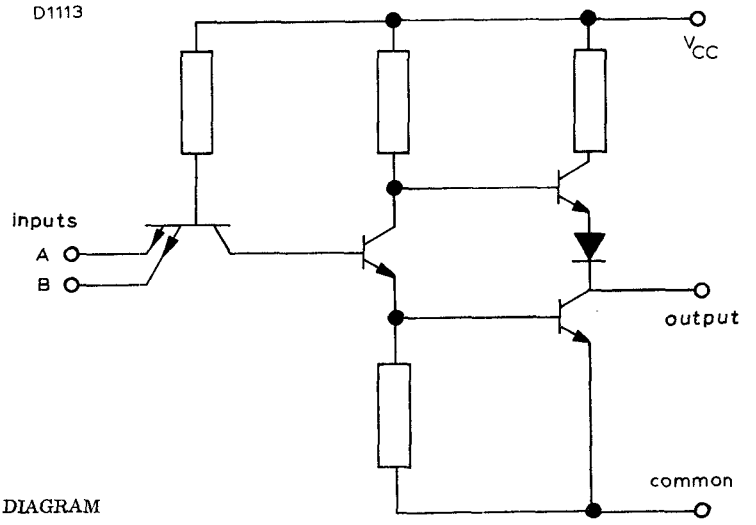


PINNING

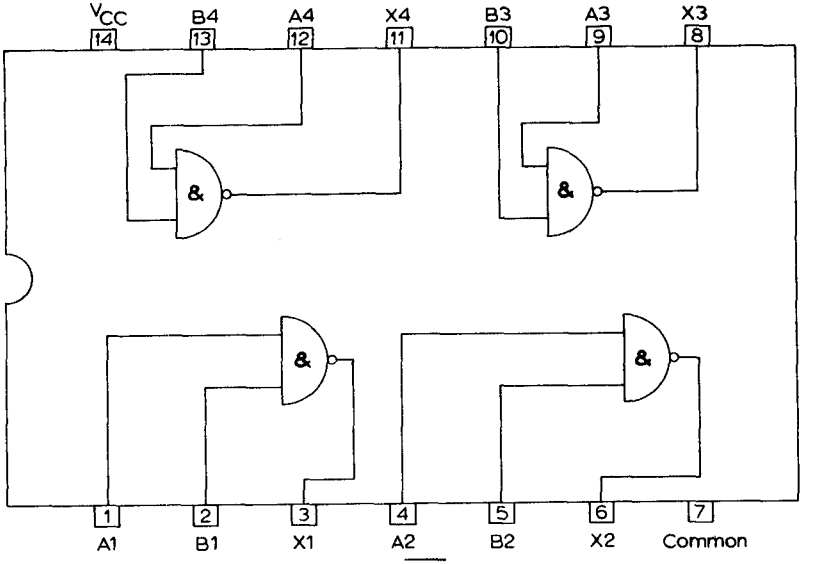
1.	Input gate 1
2.	Input gate 1
3.	Output gate 1
4.	Input gate 2
5.	Input gate 2
6.	Output gate 2
7.	Common
8.	Output gate 3
9.	Input gate 3
10.	Input gate 3
11.	Output gate 4
12.	Input gate 4
13.	Input gate 4
14.	Supply voltage

For detailed dimensions see General Explanatory Notes
For Handling Notes see General Explanatory Notes

EQUIVALENT CIRCUIT (Individual gates)



LOGIC DIAGRAM



Positive logic $\overline{X = A.B.}$