T.T.L. AND-OR-NOT GATES

FJH181
FJH181A
FJH186

Correspond to 74 Series types 7454N, 6454N

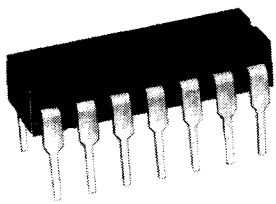
TENTATIVE DATA

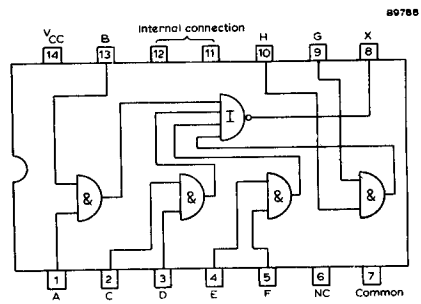
These devices are transistor-transistor logic 4-wide 2-input AND-OR-NOT gates in the FJ series of integrated circuits. The FJH181 corresponds to '74 Series' type 7454N, the FJH186 corresponds to '64 Series' type 6454N.

QUICK REFERENCE DATA			
Supply voltage (nominal)		5.0	V
Fan-out (max.)		10	
Noise immunity (typ.)		1.0	V
(min.)		0.4	V
Operating temperature range	FJH181/1A	0 to +70	^{o}C
	FJH186	-40 to +85	^{o}C
Propagation delay (typ.)		13	ns
Average power dissipation (50% duty cycle, $T_{amb}=25^{o}C$)		28.5	mW

OUTLINE

Conforms to J.E.D.E.C. TO-116 (see page 5)
FJH181 - 14-lead all plastic dual-in-line package
FJH181A - 14-lead hermetic-in-plastic dual-in-line package
FJH186 - 14-lead all plastic dual-in-line package





LOGIC FUNCTION

The logic function is AND-OR-NOT when the most positive signal is a '1'.

$$X = \overline{(A.B) + (C.D) + (E.F) + (G.H)}$$

DESIGN DATA (Maximum adverse operating conditions assumed)

		Min.	Nom.	Max.	
Temperature					
Operating ambient	FJH181/1A	0	-	70	°C
	FJH186	-40	-	85	°C
Supply					
Supply voltage	FJH181/1A	4.75	-	5.25	V
	FJH186	4.5	-	5.5	V
Supply current (output 'Low')		-	7.4	-	mA
Supply current (output 'High')		-	4.0	-	mA
Inputs					
Voltage for 'High' input state	S.N.I. = 0	2.0	-	-	V
	S.N.I. = 0.4V	2.4	-	-	V
*Current for 'High' input state (each input)		-	-	40	μA
Voltage for 'Low' input state	S.N.I. = 0	-	-	0.8	V
	S.N.I. = 0.4V	-	-	0.4	V
**Current for 'Low' input state		-	-	1.6	mA
Outputs					
Voltage for 'High' output state		2.4	-	-	V
Output resistance in 'High' output state		-	100	-	Ω
Voltage for 'Low' output state		-	-	0.4	V
Output resistance in 'Low' output state		-	12	-	Ω
Current capability in 'Low' output state		-	-	16	mA
Fan-out		-	-	10	
Performance					
Signal noise immunity		0.1	1.0	-	V
Average propagation delay time (C_L = 15pF)		-	13	-	ns

This is equivalent to a propagation delay time to the 'Low' state of 8.0ns and to the 'High' state of 18ns.

*The 'High' state normally corresponds to a voltage level between 2.4 and 5.25V.

**The 'Low' state normally corresponds to a voltage level between 0 and 0.4V.

DESIGN DATA (contd.)

Truth Table

Inputs								Resultant output
Pin 13	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 9	Pin 10	Pin 8
High	High	High	High	High	High	High	High	Low Low Low Low

Where no input logic level is specified it can either be 'High' or 'Low' without changing the output state.
All other input combinations than those above give a 'High' output.

CHARACTERISTICS (Supply voltage = 5.0V, $T_{amb} = 25^{o}C$)

		Min.	Typ.	Max.	
V_{TH} 'Low'	Input threshold voltage for 'Low' input state ($V_{out} = 2.4V$, $I_{out} = -400\mu A$, one input from each AND gate = 5.0V, other inputs measured simultaneously)	0.8*	-	-	V
V_{TH} 'High'	Input threshold voltage for 'High' input state ($I_{out} = 16mA$, $I_{out} = 0.4V$, all AND inputs 'High' simultaneously i.e. 2.0V)	-	-	2.0*	V
V_{out} 'Low'	Output voltage for 'Low' output state ($V_{in} = 2.0V$, $I_{out} = 16mA$, all AND inputs 'High' simultaneously)	-	-	0.4*	V
V_{out} 'High'	Output voltage for 'High' output state ($V_{in} = 0.8V$, $I_{out} = -400\mu A$, one input from each AND gate = 5.0V others at 0.8V)	2.4*	-	-	V
I_{in} 'Low'	Input current for 'Low' input state ($V_{in} = 0.4V$, $I_{out} = 0$)	-	-	1.6*	mA
I_{in} 'High'	Input current for 'High' input state (each input) ($V_{in} = 2.4V$, $I_{out} = 0$, other inputs = 0V)	-	-	40*	μA
I_{out} 'High'	Leakage current into the 'High' state output at $V_{out} = 6.7V$ ($V_{in} = 0$)	-	-	300	μA
I_{out} s/c 'High'	Short circuit output current for 'High' output state (All inputs $V_{in} = 0$ output grounded)	18*	-	55*	mA

CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
t_{pd0}	Propagation delay time to logical '0' level (Fan-out = 10, C_L = 15pF, other pairs of AND inputs at 0.4V)	-	8	15	ns
t_{pd1}	Propagation delay time to logical '1' level (Fan-out = 10, C_L = 15pF, other pairs of AND inputs at 0.4V)	-	18	29	ns

NOTE - C_L = total capacitance of driven gates including wiring capacitance.

*These are the characteristics which are recommended for acceptance testing purposes.

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical (with pin 7 earthed)

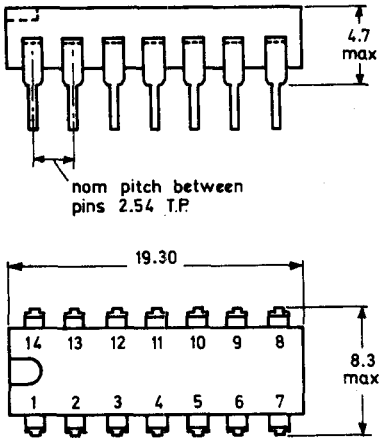
Maximum positive supply voltage (pin 14)	7.0	V
Maximum continuous input voltage (pins 1, 2, 3, 4, 5, 9, 10, 13)	5.5	V
Maximum continuous voltage applied to output (applied through $R_L \geq 270\Omega$) (Pin 8)	7.0	V
Maximum negative transient input voltage (t_p = 20ns, f = 5.0MHz, $R_s \geq 75\Omega$)	-2.0	V

Temperature

T_{stg} range	-65 to +150	°C
T_{amb} operating range FJH181/1A	0 to +70	°C
T_{amb} operating range FJH186	-40 to +85	°C

OUTLINE AND DIMENSIONS

Conforms to J.E.D.E.C. TO-116



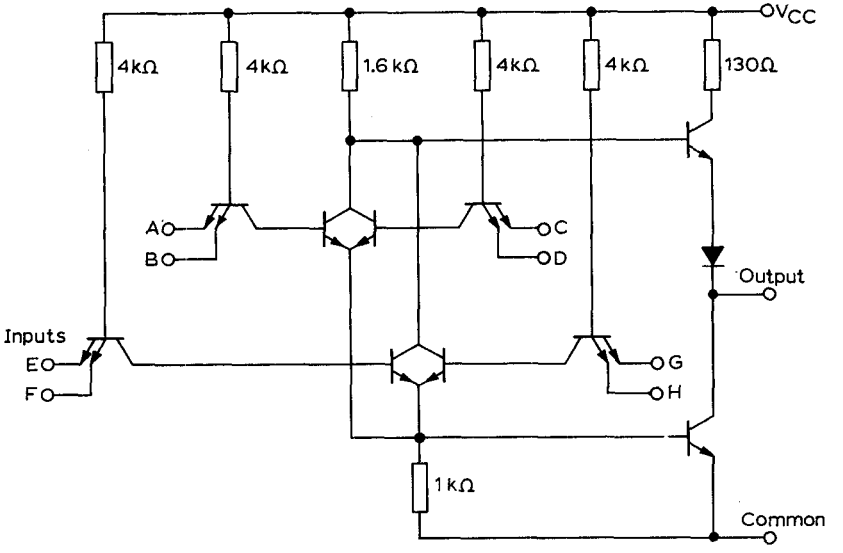
PINNING

1. A input
2. C input
3. D input
4. E input
5. F input
6. N.C.
7. Common
8. Output
9. G input
10. H input
11. } Internal
12. } connection
13. B input
14. Supply voltage

For detailed dimensions see General Explanatory Notes.
For Handling Notes see General Explanatory Notes.

NOTE - Pins 11 and 12 of the gate are internally connected and must not be used for external connections.

EQUIVALENT CIRCUIT



LOGIC DIAGRAM