T.T.L. QUADRUPLE 2-INPUT POSITIVE NAND GATES

FJH231 FJH231A

Corresponds to 74 Series type 7401N

TENTATIVE DATA

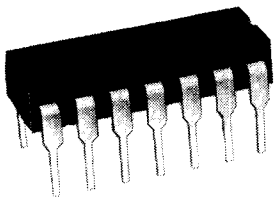
These devices are transistor-transistor logic quadruple 2-input positive NAND gates, with a single-ended open collector output transistor, in the FJ series of integrated circuits. The output may be paralleled with other similar gates to perform the wired-OR function. The FJH231 corresponds to '74 Series' type 7401N.

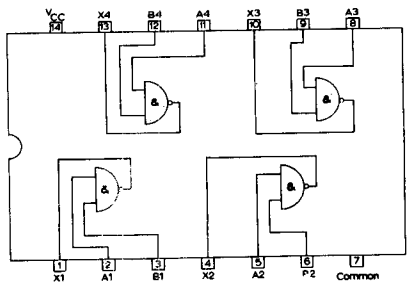
QUICK REFERENCE DATA		
Supply voltage (nominal)	5.0	V
Fan-out (max.) see table on page 4	10	
Noise immunity (typ.)	1.0	V
(min.)	0.4	V
Operating temperature range	0 to 70	^{o}C
Propagation delay (max.)	30	ns
Average power dissipation (50% duty cycle, $T_{amb}=25^{o}C$)	10	mW

Unless otherwise stated data applies to individual gates

OUTLINE

Conforms to J.E.D.E.C. TO-116 (see page 5)
FJH231 - 14-lead all plastic dual-in-line package
FJH231A - 14-lead hermetic-in-plastic dual-in-line package





LOGIC FUNCTION

The logic function of the gate is a NAND when the most positive signal voltage is a '1' and a NOR when the most positive signal voltage is a '0'. All inputs to the gate are to be 'High' in order for the output to be 'Low'. A 'Low' input to any gate input will give the output 'High'.

DESIGN DATA (Maximum adverse operating conditions assumed)

	Min.	Nom.	Max.	
Temperature				
Operating ambient	0	-	70	^{o}C
Supply				
Supply voltage	4.75	-	5.25	V
Supply current (output 'Low') per gate	-	3.0	-	mA
Supply current (output 'High') per gate	-	1.0	-	mA
Inputs				
Voltage for 'High' input state S.N.I. = 0	2.0	-	-	V
S.N.I. = 0.4V	2.4	-	-	V
*Current for 'High' input state (each input)	-	-	40	μA
Voltage for 'Low' input state S.N.I. = 0	-	-	0.8	V
S.N.I. = 0.4V	-	-	0.4	V
**Current for 'Low' input state	-	-	1.6	mA
Outputs				
Voltage for 'Low' output state	-	-	0.4	V
Output reverse current	-	-	250	μA
Current capability of 'Low' output state	-	-	16	mA
Fan-out	-	-	10	

Truth Table

Input 1	Input 2	Output
Low	Low	High
High	Low	High
Low	High	High
High	High	Low

Performance	Min.	Nom.	Max.	
Signal noise immunity	0.4	1.0	-	V
Average propagation delay time (C_L = 15pF)	-	-	30	ns

This is equivalent to a propagation delay time to the 'Low' state of 15ns and to the 'High' state of 45ns.

*The 'High' state normally corresponds to a voltage level between 2.4 and 5.25V.

**The 'Low' state normally corresponds to a voltage level between 0 and 0.4V.

CHARACTERISTICS (Supply voltage = 5.0V, $T_{amb} = 25^{o}C$)

		Min.	Typ.	Max.	
V_{TH} 'Low'	Input threshold voltage for 'Low' input state (voltage on output collector = 5.5V, collector current = 250μA)	0.8*	-	-	V
V_{TH} 'High'	Input threshold voltage for 'High' input state (I_{out} = 16mA, V_{out} = 0.4V)	-	-	2.0*	V
V_{out} 'Low'	Output voltage for 'Low' output state (V_{in} = 2.0V, I_{out} = 16mA)	-	-	0.4*	V
I_{out} 'High'	Output 'ON' current for 'High' output state (V_{in} = 0.8V, collector voltage = 5.5V)	-	-	250*	μA
I_{in} 'Low'	Input current for 'Low' input state (V_{in} = 0.4V, I_{out} = 0)	-	-	1.6*	mA
I_{in} 'High'	Input current for 'High' input state (each input) (V_{in} = 2.4V, I_{out} = 0, other input = 0V)	-	-	40*	μA
t_{pd0}	Propagation delay time to logical '0' level (collector load resistor 390Ω, C_L = 15pF)	-	-	15	ns
t_{pd1}	Propagation delay time to logical '1' level (collector load resistor 3.9KΩ, C_L = 15pF)	-	-	45	ns

NOTE - C_L = total capacitance on gate output including wiring capacitance.

*These are the characteristics which are recommended for acceptance testing purposes.

COMBINED FAN-OUT AND WIRED-OR CAPABILITIES

The open collector TTL gate, when supplied with a proper load resistor (R_L), may be paralleled with other similar TTL gates to perform the wired-OR function; and, simultaneously will drive from one to nine TTL loads. When no other open collector gates are paralleled, this gate may be used to drive ten TTL loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and I_{off} current (through paralleled outputs) will be available during a logical '1' level at the output. A minimum resistor value must be determined which will ensure that current through this resistor and current from the TTL loads will not cause the output voltage to rise above the logical '0' level even if one of the paralleled outputs is absorbing the current.

TABLE 1

FAN-OUT TO TTL LOADS	WIRED-OR OUTPUTS							
	1	2	3	4	5	6	7	1 to 7
1	8965	4814	3291	2500	2015	1688	1452	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2988	2321	1897	1604	1390	410
4	6341	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2736	2166	1793	1529	1333	575
6	5306	3513	2626	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1699	1460	1280	958
8	4561	3170	2429	1969	1656	X	X	1437
9	4262	3023	X	X	X	X	X	2875
10	4000	X	X	X	X	X	X	4000*
	Maximum							Min.
	Load resistor value in ohms							

X - Not recommended or not possible

* - The theoretical value is ∞. See explanation in text below.

All values shown in the table are based on:

Logical '1' conditions: $V_{CC} = 5.0v$, $V_{out(1)}$ required $= 2.4V$

Logical '0' conditions: $V_{CC} = 5.0V$, $V_{out(0)}$ required $= 0.4V$

DRIVING TTL LOADS AND COMBINING OUTPUTS

Table 1 provides minimum and maximum resistor values, calculated as above, for driving one to ten TTL loads and wired-OR connecting two to seven parallel outputs. Each value shown for wired-OR output one is determined by the fan-out plus the leakage of a single output transistor. Extension beyond seven wired-OR connections is permitted with fan-outs of seven or less if a valid minimum and maximum R_L is possible. When fanning-out to ten TTL loads the calculation for the minimum value of R_1 indicates that an infinite resistance should be used ($V_{RL} - 0 = \infty$), however, the use of a 4kΩ resistor in this case will satisfy the logical '1' conditions and limit the logical '0' voltage to less than 0.43V.

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RATINGS

Limiting values of operation according to the absolute maximum system

Electrical

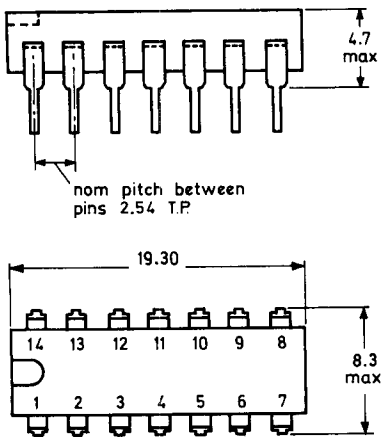
Maximum positive supply voltage (pin 14)	7.0	V
Maximum continuous input voltage (pins 2, 3, 5, 6, 8, 9, 11 and 12)	5.5	V
Maximum continuous voltage applied to output (applied through $R_L \geq 270\Omega$) (Pins 1, 4, 10, 13)	7.0	V
Maximum negative transient input voltage (t_p=20ns, f=5.0MHz, $R_s \geq 75\Omega$)	-2.0	V

Temperature

T_{stg}	-65 to +150	°C
T_{amb} operating	0 to +70	°C

OUTLINE AND DIMENSIONS

Conforms to J.E.D.E.C. TO-116



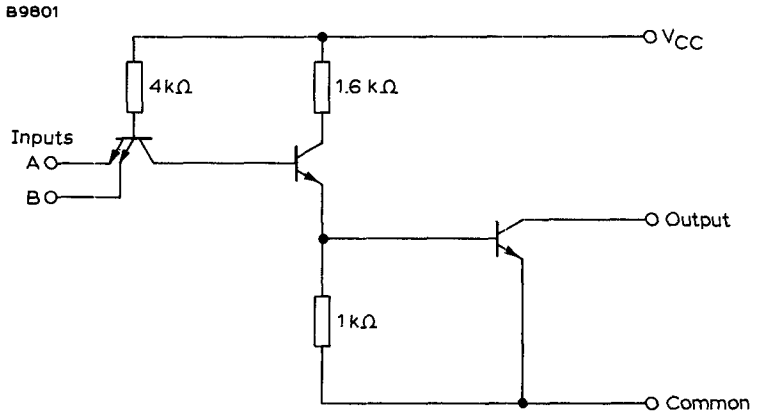
PINNING

1.	Output gate 1
2.	A input gate 1
3.	B input gate 1
4.	Output gate 2
5.	A input gate 2
6.	B input gate 2
7.	Common
8.	A input gate 3
9.	B input gate 3
10.	Output gate 3
11.	A input gate 4
12.	B input gate 4
13.	Output gate 4
14.	Supply voltage

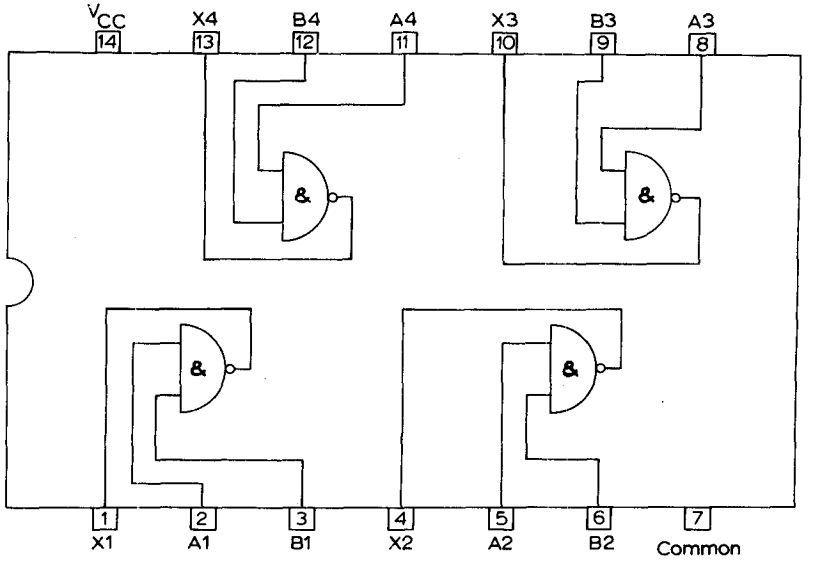
For detailed dimensions see General Explanatory Notes

For Handling Notes see General Explanatory Notes

EQUIVALENT CIRCUIT (Individual gates)



LOGIC DIAGRAM



Positive logic $X = \overline{A.B}$