T.T.L. EDGE-TRIGGERED DUAL D-TYPE FLIP-FLOPS

FJJ131
FJJ131A
FJJ136

Correspond to 74 Series types 7474N, 6474N

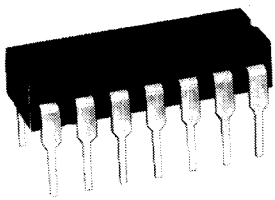
TENTATIVE DATA

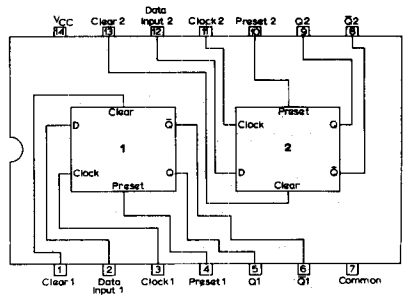
These devices are transistor-transistor logic edge-triggered dual D-type flip-flops, with direct, clear and preset inputs and complementary Q and $\overline{Q}$ outputs, in the FJ series of integrated circuits. The FJJ131 corresponds to '74 Series' type 7474N, the FJJ136 corresponds to '64 Series' type 6474N.

QUICK REFERENCE DATA		
Supply voltage (nominal)	5.0	V
Max. clock rate	15	MHz
Fan-out	10	
Noise immunity (typ.)	1.0	V
(min.)	0.4	V
Total dissipation (per flip-flop)	42.5	mW

OUTLINE

Conforms to J.E.D.E.C. TO-116 (see page 6)
FJJ131 - 14-lead all plastic dual-in-line package
FJJ131A - 14-lead hermetic-in-plastic dual-in-line package
FJJ136 - 14-lead all plastic dual-in-line package





LOGIC FUNCTION

The logic function of the 'D' type flip-flop is that the input information on the 'D' input is transferred to the 'Q' output on the positive edge of the clock pulse. After the clock input threshold voltage has been exceeded the 'D' (data) input is locked out.

DESIGN DATA (Maximum adverse operating conditions assumed)

			Min.	Nom.	Max.	
Temperature						
Operating ambient	FJJ131/1A		0	-	70	°C
	FJJ136		-40	-	85	°C
Supply						
Supply voltage	FJJ131/1A		4.75	-	5.25	V
	FJJ136		4.5	-	5.5	V
Supply current with Clock and 'D' inputs at ground (each bistable)			-	8.5	-	mA
Inputs						
Voltage for 'High' input state						
All inputs		S.N.I. = 0	2.0	-	-	V
		S.N.I. = 0.4V	2.4	-	-	V
*Current for 'High' input state						
'D' inputs			-	-	40	μA
Preset or Clock inputs			-	-	80	μA
Clear input			-	-	120	μA
Voltage for 'Low' input state		S.N.I. = 0	-	-	0.8	V
		S.N.I. = 0.4V	-	-	0.4	V
**Current for 'Low' input state						
Preset or 'D' inputs			-	-	1.6	mA
Clear or Clock inputs			-	-	3.2	mA
Outputs						
Voltage for 'High' output state			2.4	-	-	V
Voltage for 'Low' output state			-	-	0.4	V
Output resistance in 'High' output state			-	100	-	Ω
Output resistance in 'Low' output state			-	12	-	Ω
Current capability at 'Low' output state			-	-	16	mA
Fan-out						
Preset or 'D' inputs			-	-	10	
Clear or Clock inputs			-	-	5	
Performance						
Signal noise immunity			0.4	1.0	-	V
Average propagation delay time (Clock input, $C_L = 15pF$)			-	24	-	ns

This is equivalent to a propagation delay time to the 'Low' state of 20ns and to the 'High' state of 28ns.

*The 'High' state normally corresponds to a voltage level between 2.4 and 5.25V.

**The 'Low' state normally corresponds to a voltage level between 0 and 0.4V.

DESIGN DATA (cont'd)

Truth table (each flip-flop)

t_n	t_{n+1}	
Input	Output	
Pin 2/12	Pin 5/9	Pin 6/8
Low	Low	High
High	High	Low

Notes

1. t_n = bit time before clock pulse
2. t_{n+1} = bit time after rising edge of clock pulse

CHARACTERISTICS

$T_{amb} = 25^{\circ}C$, Supply voltage = 5.0V, each flip-flop

Bistable must be set with Q to '0' prior to making these tests

		Min.	Typ.	Max.	
V_{TH} 'Low'	Input threshold voltage for 'Low' input state (Preset and Clear inputs) ($I_{out} = -400\mu A$, $V_{preset} = 2.0V$, $V_{clear} = 0.8V$)	0.8*	-	-	V
V_{TH} 'High'	Input threshold voltage for 'High' input state (Preset and Clear inputs) ($I_{out} = 16mA$, $V_{out} = 400mV$, $V_{preset} = 2.0V$, $V_{clear} = 0.8V$)	-	-	2.0*	V
V_{out} 'Low'	Output voltage for 'Low' output state (Preset and Clear inputs) ($I_{out} = 16mA$, $V_{preset} = 2.0V$, $V_{clear} = 0.8V$)	-	-	0.4*	V
V_{out} 'High'	Output voltage for 'High' output state (Preset and Clear inputs) ($I_{out} = -400\mu A$, $V_{preset} = 0.8V$, $V_{clear} = 2.0V$, V_{clock} and $V_{data} = 2.0V$)	2.4*	-	-	V
I_{in} 'Low'	Data input current for 'Low' input state ($V_{data} = 0.4V$, $V_{preset} = 0V$, V_{clear} and $V_{clock} = 4.5V$)	-	-	1.6*	mA

CHARACTERISTICS (cont'd)

		Min.	Typ.	Max.	
I_{in} 'Low'	Preset input current for 'Low' input state (V_{preset} = 0.4V, V_{data} = 0, V_{clear} and V_{clock} = 4.5V)	-	-	1.6*	mA
I_{in} 'Low'	Clock input current for 'Low' input state (V_{clock} = 0.4V, V_{data} = 0V, V_{clear} and V_{preset} = 4.5V)	-	-	3.2*	mA
I_{in} 'Low'	Clear input current for 'Low' input state (V_{clear} = 0.4V, V_{data} and V_{clock} = 4.5V)	-	-	3.2*	mA
I_{in} 'High'	Data input current for 'High' input state (V_{data} = 2.4V, V_{clear} = 0, V_{clock} = 4.5V)	-	-	40*	μA
I_{in} 'High'	†Preset input current for 'High' input state (V_{preset} = 2.4V, V_{clear} and V_{data} = 4.5V, output Q 'High'	-	-	80*	μA
I_{in} 'High'	Clock input current for 'High' input state (V_{clock} = 2.4V, V_{clear} = 0)	-	-	80*	μA
I_{in} 'High'	†Clear input current for 'High' input state (V_{clear} = 2.4V, V_{clock} and V_{data} = 0, output Q 'High'	-	-	80*	μA
I_{out} s/c "High'	Short circuit output current for 'High' output state (V_{preset} = 0, output Q grounded)	18*	-	57*	mA

*These are the characteristics which are recommended for acceptance testing purposes.

†The Preset or Clear inputs are momentarily grounded to achieve correct output state before commencing measurement.

Switching characteristics (C_L = 15pF, Fan-out = 10)

	Min.	Typ.	Max.	
Set up time	20	-	-	ns
Hold time	5	-	-	ns
Clock frequency	15	25	-	MHz
Clock pulse width	30	-	-	ns

CHARACTERISTICS (cont'd)

Switching characteristics (cont'd)

		Min.	Typ.	Max.	
t_{pd0}	Propagation delay time to logical '0' level from Clock to output	10	-	50	ns
t_{pd1}	Propagation delay time to logical '1' level from Clock to output	10	-	35	ns
t_{pd0}	Propagation delay time to logical '0' level from Clear or Preset to output	-	-	40	ns
t_{pd1}	Propagation delay time to logical '1' level from Clear or Preset to output	-	-	25	ns

Note:- C_L = Total capacitance of driven gates including wiring capacitance.

Switching waveforms - See separate sheet

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

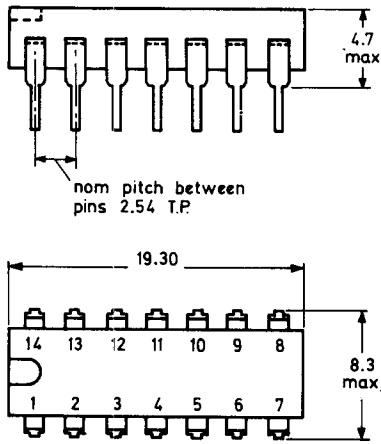
Maximum positive supply voltage (pin 14)	7.0	V
Maximum continuous input voltage (pins 1, 2, 3, 4, 10, 11, 12, 13)	5.5	V
Maximum negative transient input voltage (t_p = 20ns, f = 5.0MHz, $R_s \geq 75\Omega$)	-2.0	V
Minimum width of clock pulse	30	ns
Minimum width of preset or clear pulse	25	ns

Temperature

T_{stg} min.		-65	°C
T_{stg} max.		150	°C
T_{amb} operating range	FJJ131/1A	0 to +70	°C
T_{amb} operating range	FJJ136	-40 to +85	°C

OUTLINE AND DIMENSIONS

Conforms to J.E.D.E.C. TO-116



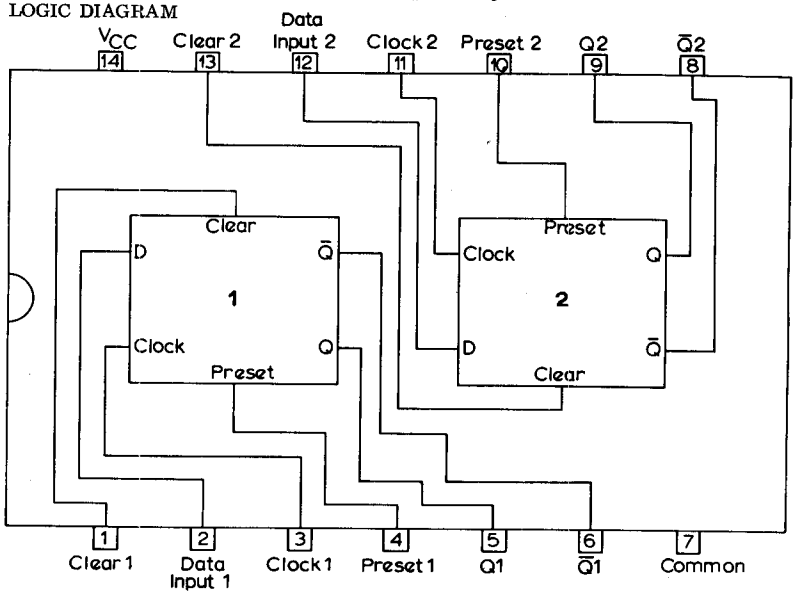
PINNING

1. Clear input circuit 1
2. 'D' input circuit 1
3. Clock input circuit 1
4. Preset input circuit 1
5. Q output circuit 1
6. $\overline{Q}$ output circuit 1
7. Common
8. $\overline{Q}$ output circuit 2
9. Q output circuit 2
10. Preset input circuit 2
11. Clock input circuit 2
12. 'D' input circuit 2
13. Clear input circuit 2
14. Supply voltage

For detailed dimensions see General Explanatory Notes

For Handling Notes see General Explanatory Notes

LOGIC DIAGRAM



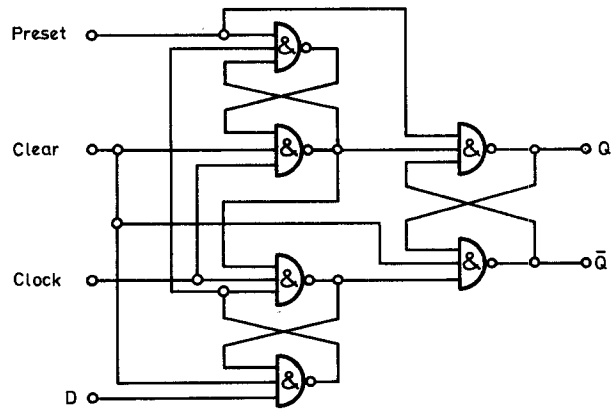
a. 'Low' input to preset sets Q to logical '1'

b. 'Low' input to clear sets Q to logical '0'

c. Clear and preset inputs dominate regardless of clock and 'D' inputs.

Positive logic

FUNCTIONAL BLOCK DIAGRAM (each flip-flop)



SCHEMATIC (each flip-flop)